

FORM PTO-1449 \*

## INFORMATION DISCLOSURE STATEMENT

**COPY**

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>SP</i>	A217	2003/0227057	12/01/2003	Lochtefeld et al.			10/04/2002
	A218	2003/0230778 A1	12/18/2003	Park et al.			01/30/2003
	A219	2003/0232467 A1	12/18/2003	Anderson et al.			05/29/2003
	A220	2004/0005740	01/01/2004	Lochtefeld et al.			06/06/2003
	A221	2004/0007724 A1	01/15/2004	Murthy et al.			07/12/2002
	A222	2004/0009649 A1	01/15/2004	Kub et al.			05/20/2003
	A223	2004/0012037 A1	01/22/2004	Venkatesan et al.			07/18/2002
	A224	2004/0012075 A1	01/22/2004	Bedell et al.			07/16/2002
	A225	2004/0014304 A1	01/22/2004	Bhattacharyya			07/18/2002
	A226	2004/0018699 A1	01/29/2004	Boyd et al.			07/24/2002
	A227	2004/0031979	02/19/2004	Lochtefeld et al.			06/06/2003
	A228	2004/0031990 A1	02/19/2004	Jin et al.			08/16/2002
	A229	2004/0041174 A1	03/04/2004	Okihara			03/21/2003
	A230	2004/0041210 A1	03/04/2004	Mouli			09/02/2003
	A231	2004/0048091 A1	03/11/2004	Sato et al.			09/04/2003
	A232	2004/0048454 A1	03/11/2004	Sakaguchi			09/04/2003
	A233	2004/0051140 A1	03/18/2004	Bhattacharyya			09/12/2002
<i>✓</i>	A234	2004/0053477 A1	03/18/2004	Ghyselen et al.			07/09/2003

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<i>SP</i>	B1	41 01 167	07/23/1992	DE				No	No
	B2	0 514 018	11/19/1992	EP				No	Yes
	B3	0 587 520	03/16/1994	EP				No	Yes
	B4	0 683 522	11/22/1995	EP				No	Yes
	B5	0 828 296	03/11/1998	EP				No	Yes
	B6	0 829 908	03/18/1998	EP				No	Yes
<i>✓</i>	B7	0 838 858	04/29/1998	EP				No	No

EXAMINER

*Sflu*

DATE CONSIDERED

*10/16/07*

\*: Pages 9-17 only.

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

**COPY**

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLAS S	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<i>sk</i>	B8	1 020 900	07/19/2000	EP				No	Yes
	B9	1 174 928	01/23/2002	EP				No	Yes
	B10	2 342 777	04/19/2000	GB				Yes	Yes
	B11	4-307974	10/30/1992	JP				No	No
	B12	5-166724	07/03/1993	JP				No	Abstract Only
	B13	6-177046	06/24/1994	JP				No	Abstract Only
	B14	7-106446	04/21/1995	JP				No	No
	B15	7-240372	09/12/1995	JP				No	Abstract Only
	B16	10-270685	10/09/1998	JP				No	Yes
	B17	11-233744	08/27/1999	JP				No	No
	B18	2000-021783	01/21/2000	JP				No	Yes
	B19	2000-31491	01/28/2000	JP				No	No
	B20	2001319935	05/11/2000	JP				Yes	Yes
	B21	2002-076334	03/15/2002	JP				No	Yes
	B22	2002-164520	06/07/2002	JP				No	Yes
	B23	2002-289533	10/04/2002	JP				No	Yes
	B24	WO 98/59365	12/30/1998	PCT				No	Yes
	B25	WO 99/53539	10/21/1999	PCT				No	Yes
	B26	WO 00/48239	08/17/2000	PCT				No	Yes
	B27	WO 01/54202	07/26/2001	PCT				No	Yes
	B28	WO 01/99169A2	12/27/2001	PCT				No	Yes
	B29	WO 02/15244 A2	02/21/2002	PCT				No	Yes
	B30	WO 02/27783 A1	04/04/2002	PCT				No	Yes
<i>✓</i>	B31	WO 02/071495A1	09/12/2002	PCT				No	Yes

EXAMINER

*SPH*

DATE CONSIDERED

*10/16/07*

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

COPY

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLAS S	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<i>SL</i>	B32	WO 02/082514 A1	10/17/2002	PCT				No	Yes
	B33	WO 00/54338	09/14/2000	WO				No	Yes
	B34	WO 01/022482	03/29/2001	WO				No	Yes
	B35	WO 01/93338	12/06/2001	WO				No	Yes
	B36	WO 02/13262	02/14/2002	WO				No	Yes
	B37	WO 02/47168	06/13/2002	WO				No	Yes
	B38	WO 02/071488	09/12/2002	WO				No	Yes
	B39	WO 02/071491	09/12/2002	WO				No	Yes
	B40	WO 04/006311 A2	01/15/2004	WO			07/09/2003		YES
	B41	WO 04/006326 A1	01/15/2004	WO			07/09/2003		YES
	B42	WO 04/006327 A2	01/15/2004	WO			07/09/2003		YES
	B43	WO 04/019403 A2	03/04/2004	WO			08/26/2003		YES
<i>✓</i>	B44	WO 04/019404 A2	03/04/2004	WO			08/26/2003		YES

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
<i>SL</i>	C1	"2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," IBM Technical Disclosure Bulletin, Vol. 35, No. 4B (September 1992) pp. 136-140.
	C2	Armstrong et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEDM Technical Digest</u> (1995) pp. 761-764.
	C3	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices", Ph.D Thesis, Massachusetts Institute of Technology (1999) pp. 1-154.
	C4	Augusto et al., "Proposal for a New Process Flow for the Fabrication of Silicon-Based Complementary MOD-MOSFETs without Ion Implantation," <u>Thin Solid Films</u> , Vol. 294, No. 1-2 (1997) pp. 254-258.
<i>✓</i>	C5	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," <u>Modern Physics Letters B</u> (2001) (abstract).

EXAMINER

*SL*

DATE CONSIDERED

*10/16/07*

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

COPY

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.  
INIT.

OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)

- |     |   |
|-----|---|
| C6  | Borenstein et al., "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," <u>Proceedings of the 1999 12<sup>th</sup> IEEE International Conference on Micro Electro Mechanical Systems (MEMS)</u> (January 17-21, 1999) pp. 205-210. |
| C7  | Bouillon et al., "Search for the optimal channel architecture for 0.18/0.12 $\mu$ m bulk CMOS Experimental study," <u>IEEE</u> (1996) pp. 21.2.1-21.2.4.  |
| C8  | Bruel et al., "©SMART CUT: A Promising New SOI Material Technology," <u>Proceedings 1995 IEEE International SOI Conference</u> (October 1995) pp. 178-179.  |
| C9  | Bruel, "Silicon on Insulator Material Technology," <u>Electronic Letters</u> , Vol. 13, No. 14 (July 6, 1995) pp. 1201-1202.  |
| C10 | Bufler et al., "Hole transport in strained Si <sub>1-x</sub> Ge <sub>x</sub> alloys on Si <sub>1-y</sub> Ge <sub>y</sub> substrates," <u>Journal of Applied Physics</u> , Vol. 84, No. 10 (November 15, 1998) pp. 5597-5602.                        |
| C11 | Burghartz et al., "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," <u>IEEE Transactions on Microwave Theory and Techniques</u> , Vol. 44, No. 1 (January 1996) pp. 100-104.                             |
| C12 | Carlin et al., "High Efficiency GaAs-on-Si Solar Cells with High Voc Using Graded GeSi Buffers," <u>IEEE</u> (2000) pp. 1006-1011   |
| C13 | Chang et al., "Selective Etching of SiGe/Si Heterostructures," <u>Journal of the Electrochemical Society</u> , No. 1 (January 1991) pp. 202-204.  |
| C14 | Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 7 (July 2001) pp. 321-323.   |
| C15 | Cheng et al., "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," <u>Journal of Electronic Materials</u> , Vol. 30, No. 12 (2001) pp. L37-L39.  |
| C16 | Cullis et al., "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," <u>Journal of Vacuum Science and Technology A</u> , Vol. 12, No. 4 (July/August 1994) pp. 1924-1931.                                 |
| C17 | Currie et al., "Carrier mobilities and process stability of strained Si n- and p-MOSFETs on SiGe virtual substrates," <u>J. Vac. Sci. Technol. B</u> , Vol. 19, No. 6 (Nov/Dec 2001) pp. 2268-2279.   |
| C18 | Currie et al., "Controlling Threading Dislocation in Ge on Si Using Graded SiGe Layers and Chemical-Mechanical Polishing," <u>Applied Physics Letters</u> , vol. 72 No. 14 (April 6, 1998) pp. 1718-1720.   |
| C19 | Eaglesham et al., "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," <u>Physical Review Letters</u> , Vol. 64, No. 16 (April 16, 1990) pp. 1943-1946.   |
| C20 | Feijoo et al., "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," <u>Journal of Electronic Materials</u> , Vol. 23, No. 6 (June 1994) pp. 493-496.                                 |
| C21 | Fischetti et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," <u>J. Appl. Phys.</u> , Vol. 80, No. 4 (August 15, 1996) pp. 2234-2252.   |

EXAMINER

DATE CONSIDERED

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

COPY

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.  
INIT.

OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)

- C22 Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electron mobility in thin-oxide structures," Journal of Applied Physics, Vol. 89, No. 2 (January 15, 2001) pp. 1232-1250.
- C23 Fitzgerald et al., "Dislocation dynamics in relaxed graded composition semiconductors," Materials Science and Engineering B67 (1999) pp. 53-61.
- C24 Fitzgerald et al., "Relaxed  $\text{Ge}_x\text{Si}_{1-x}$  structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," AT&T Bell Laboratories, Murray Hill, NJ 07974 (1992) American Vacuum Society, pp. 1807-1819.
- C25 Fitzgerald et al., "Totally Relaxed  $\text{Ge}_x\text{Si}_{1-x}$  Layers with Low Threading Dislocation Densities Grown on Si Substrates," Applied Physics Letters, Vol. 59, No. 7 (August 12, 1991) pp. 811-813.
- C26 Garone et al., "Silicon vapor phase epitaxial growth catalysis by the presence of germane," Applied Physics Letters, Vol. 56, No. 13 (March 26, 1990) pp. 1275-1277.
- C27 Godbey et al., (1990) "Fabrication of Bond and Etch-Back Silicon Insulator Using a Strained  $\text{Si}_{0.7}\text{Ge}_{0.3}$  Layer as an Etch Stop," Journal of the Electrical Society, Vol. 137, No. 10 (October 1990) pp. 3219-3223.
- C28 Gray and Meyer, "Phase-Locked Loops," Analysis and Design of Analog Integrated Circuits (1984) pp. 605-632.
- C29 Grützmacher et al., "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," Applied Physics Letters, Vol. 63, No. 18 (November 1, 1993) pp. 2531-2533.
- C30 Hackbarth et al., "Alternatives to thick MBE-grown relaxed SiGe buffers," Thin Solid Films, Vol. 369, No. 1-2 (July 2000) pp. 148-151.
- C31 Hackbarth et al., "Strain relieved SiGe buffers for Si-based heterostructure field-effect transistors," Journal of Crystal Growth, Vol. 201/202 (1999) pp. 734-738.
- C32 Herzog et al., "SiGe-based FETs: buffer issues and device results," Thin Solid Films, Vol. 380 (2000) pp. 36-41.
- C33 Höck et al., "Carrier mobilities in modulation doped  $\text{Si}_{1-x}\text{Ge}_x$  heterostructures with respect to FET applications," Thin Solid Films, Vol. 336 (1998) pp. 141-144.
- C34 Höck et al., "High hole mobility in  $\text{Si}_{0.17}\text{Ge}_{0.83}$  channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," Applied Physics Letters, Volume 76, No. 26 (June 26, 2000) pp. 3920-3922.
- C35 Höck et al., "High performance 0.25  $\mu\text{m}$  p-type Ge/SiGe MODFETs," Electronics Letters, Vol. 34, No. 19 (September 17, 1998) pp. 1888-1889.
- C36 Huang et al., (2001) "Carrier Mobility enhancement in strained Si-on-insulator fabricated by wafer bonding," 2001 Symposium on VLSI Technology, Digest of Technical Papers, pages 57-58
- C37 Huang et al., "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," Applied Physics Letters, Vol. 76, No. 19 (May 8, 2000) pp. 2680-2682.
- C38 Huang et al., "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits," IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, July, 1998, pp. 1023-1036.

EXAMINER

DATE CONSIDERED

10/16/07

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

COPY

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.  
INIT.

OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)

- C39 IBM Technical Disclosure Bulletin, Volume 32, No. 8A, January 1990, "Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates", pp. 330-331.
- C40 Ishikawa et al., "Creation of Si-Ge-based SIMOX structures by low energy oxygen implantation," Proceedings 1997 IEEE International SOI Conference (October 1997) pp. 16-17.
- C41 Ishikawa et al., "SiGe-on-insulator substrate using SiGe alloy grown Si(001)," Applied Physics Letters, Vol. 75, No. 7 (August 16, 1999) pp. 983-985.
- C42 Ismail et al., "Modulation-doped n-type Si/SiGe with inverted interface," Appl. Phys. Lett., Vol. 65, No. 10 (September 5, 1994) pp. 1248-1250.
- C43 Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington, D.C. (December 10, 1995) pp. 20.1.1-20.1.4.
- C44 Kearney et al., "The effect of alloy scattering on the mobility of holes in a  $\text{Si}_{1-x}\text{Ge}_x$  quantum well," Semicond. Sci Technol., Vol. 13 (1998) pp. 174-180.
- C45 Kim et al., "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier," IEEE Microwave and Guided Wave Letters, Vol. 8, No. 8 (August 1998) pp. 293-295.
- C46 Koester et al., "Extremely High Transconductance  $\text{Ge/Si}_{0.4}\text{Ge}_{0.6}$  p-MODFET's Grown by UHV-CVD," IEEE Electron Device Letters, Vol. 21, No. 3 (March 2000) pp. 110-112.
- C47 König et al., "Design Rules for n-Type SiGe Hetero FETs," Solid State Electronics, Vol. 41, No. 10 (1997), pp. 1541-1547.
- C48 König et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters, Vol. 14, No. 4 (April 1993) pp. 205-207.
- C49 König et al., "SiGe HBTs and HFETs," Solid-State Electronics, Vol. 38, No. 9 (1995) pp. 1595-1602.
- C50 Kummer et al., "Low energy plasma enhanced chemical vapor deposition," Materials Science and Engineering B89 (2002) pp. 288-295.
- C51 Kuznetsov et al., "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," J. Vac. Sci. Technol., B 13(6) (November/December 1995) pp. 2892-2896.
- C52 Langdo et al., (2002) "Preparation of Novel SiGe-free Strained Si on Insulator Substrates" IEEE International SOI Conference, pages 211-212 (XP002263057)
- C53 Larson, "Integrated Circuit Technology Options for RFIC's - Present Status and Future Directions," IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, March 1998, pp. 387-399.
- C54 Lee et al., "CMOS RF Integrated Circuits at 5 GHz and Beyond," Proceedings of the IEEE, Vol. 88, No. 10 (October 2000) pp. 1560-1571.
- C55 Lee et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on  $\text{Si}_{1-x}\text{Ge}_x$ /Si virtual substrates," Applied Physics Letters, Vol. 79, No. 20 (November 12, 2001) pp. 3344-3346.
- C56 Lee et al., "Strained Ge channel p-type MOSFETs fabricated on  $\text{Si}_{1-x}\text{Ge}_x$ /Si virtual substrates," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A1.9.1-A1.9.5.

EXAMINER

*S. Lee*

DATE CONSIDERED

10/16/07

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

**COPY**

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.  
INIT.

OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)

- C57 Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A3.10.1-A3.10.6.
- C58 Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," Journal of Applied Physics, Vol. 90, No. 6 (September 15, 2001) pp. 2730-2736.
- C59 Leitz et al., "Hole mobility enhancements in strained Si/Si<sub>1-y</sub>Ge<sub>y</sub> p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si<sub>1-x</sub>Ge<sub>x</sub> (x<y) virtual substrates," Applied Physics Letters, Vol. 79, No. 25 (December 17, 2001) pp. 4246-4248.
- C60 Li et al., "Design of high speed Si/SiGe heterojunction complementary metal-oxide-semiconductor field effect transistors with reduced short-channel effects," J. Vac. Sci. Technol., Vol. 20 No.3 (May/June 2002) pp. 1030-1033.
- C61 Lu et al., "High Performance 0.1  $\mu$ m Gate-Length P-Type SiGe MODFET's and MOS-MODFET's," IEEE Transactions on Electron Devices, Vol. 47, No. 8 (August 2000) pp. 1645-1652.
- C62 Maiti et al., "Strained-Si heterostructure field effect transistors," Semicond. Sci. Technol., Vol. 13 (1998) pp. 1225-1246.
- C63 Maszara, "Silicon-On-Insulator by Wafer Bonding: A Review," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 341-347.
- C64 Meyerson et al., "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," Applied Physics Letters, Vol. 53, No. 25 (December 19, 1988) pp. 2555-2557.
- C65 Mizuno et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS-Electron/Hole Mobility Enhancement," "2000 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, (June 13-15), IEEE New York, NY, pp. 210-211.
- C66 Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE Electron Device Letters, Vol. 21, No. 5 (May 2000) pp. 230-232.
- C67 Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE IDEM Technical Digest (1999) pp. 934-936.
- C68 Nayak et al., "High-Mobility Strained-Si PMOSFET's," IEEE Transactions on Electron Devices, Vol. 43, No. 10 (October 1996) pp. 1709-1716.
- C69 O'Neill et al., "SiGe Virtual substrate N-channel heterojunction MOSFETS," Semicond. Sci. Technol., Vol. 14 (1999) pp. 784-789.
- C70 Ota, Y. et al., "Application of heterojunction FET to power amplifier for cellular telephone," Electronics Letters, Vol. 30 No. 11 (May 26, 1994) pp. 906-907.
- C71 Papananos, "Low Noise Amplifiers in MOS Technologies," and "Low Noise Tuned-LC Oscillator," Radio-Frequency Microelectronic Circuits for Telecommunication Applications (1999) pp. 115-117, 188-193.
- C72 Parker et al., "SiGe heterostructure CMOS circuits and applications," Solid State Electronics, Vol. 43 (1999) pp. 1497-1506.

EXAMINER

DATE CONSIDERED

FORM PTO - 1449

## INFORMATION DISCLOSURE STATEMENT

**COPY**

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

## OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.  
INIT.

OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)

- |     |   |
|-----|---|
| C73 | Ransom et al., "Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 38, No. 12 (December 1991) pp. 2695.                                 |
| C74 | Reinking et al., "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," <u>Electronics Letters</u> , Vol. 35, No. 6 (March 18, 1999) pp. 503-504.  |
| C75 | Rim et al., "Enhanced Hole Mobilities in Surface-channel Strained-Si p-MOSFETs"; <u>IEDM</u> , 1995, pp. 517-520.   |
| C76 | Rim et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's"; <u>IEEE Transactions on Electron Devices</u> , Vol. 47, No. 7 (July 2000) pp. 1406-1415.                               |
| C77 | Rim, "Application of Silicon-Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field-Effect Transistors", Ph.D. Thesis, Stanford University (1999) pp. 1-184.                       |
| C78 | Robbins et al., "A model for heterogeneous growth of Si <sub>1-x</sub> Ge <sub>x</sub> films for hydrides," <u>Journal of Applied Physics</u> , Vol. 69, No. 6 (March 15, 1991) pp. 3729-3732.          |
| C79 | Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEEE Trans. Electron Devices</u> (August 1996) pp. 1224-1232.                                  |
| C80 | Sakaguchi et al., "ELTRAN® by Splitting Porous Si Layers," Proc. 195 <sup>th</sup> Int. SOI Symposium, Vol. 99-3, <u>Electrochemical Society</u> (1999) pp. 117-121.                                    |
| C81 | Schäffler, "High-Mobility Si and Ge Structures," <u>Semiconductor Science and Technology</u> , Vol. 12 (1997) pp. 1515-1549.  |
| C82 | Sugimoto et al., "A 2V, 500 MHz and 3V, 920 MHz Low-Power Current-Mode 0.6 $\mu$ m CMOS VCO Circuit", <u>IEICE Trans. Electron.</u> , Vol.E82-C, No. 7 (July 1999) pp. 1327-1329.                       |
| C83 | Tement et al., "Metal Gate Strained Silicon MOSFETs for Microwave Integrated Circuits", <u>IEEE</u> (October 2000) pp. 38-43.   |
| C84 | Tsang et al., "Measurements of alloy composition and strain in thin Ge <sub>x</sub> Si <sub>1-x</sub> layers," <u>J. Appl. Phys.</u> , Vol. 75 No. 12 (June 15, 1994) pp. 8098-8108.                    |
| C85 | Tweet et al., "Factors determining the composition of strained GeSi layers grown with disilane and germane," <u>Applied Physics Letters</u> , Vol. 65, No. 20 (November 14, 1994) pp. 2579-2581.        |
| C86 | Usami et al., "Spectroscopic study of Si-based quantum wells with neighboring confinement structure," <u>Semicon. Sci. Technol.</u> (1997) (abstract).  |
| C87 | Welser et al., "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," <u>IEEE Electron Device Letters</u> , Vol. 15, No. 3 (March 1994) pp. 100-102. |
| C88 | Welser et al., "Evidence of Real-Space Hot-Electron Transfer in High Mobility, Strained-Si Multilayer MOSFETs," <u>IEEE IDEM Technical Digest</u> (1993) pp. 545-548.                                   |
| C89 | Welser et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," <u>IEEE IDEM Technical Digest</u> (1992) pp. 1000-1002.                                 |
| C90 | Welser, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors," Ph.D. Thesis, Stanford University (1994) pp. 1-205.     |
| C91 | Wolf et al., "Silicon Processing for the VLSI Era," Vol. 1 <u>Process Technology</u> (1986) pp. 384-386.  |

EXAMINER

DATE CONSIDERED

10/16/07






8-6-07

Used in Lieu of PTO/SB/08A/B  
(Based on PTO 04-07 version)

Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>			<b>Complete If Known</b>		
			Application Number	10/802,186-Conf. #3869	
			Filing Date	March 17, 2004	
			First Named Inventor	Cheng	
			Art Unit	2811	
			Examiner Name	Shouxiang Hu	
Sheet	1	of	3	Attorney Docket Number	ASC-025DV2C1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	A275*	US-20020167048-A1	11-14-2002	Tweet et al.	
	A276*	US-20030027381-A1	02-06-2003	Buynoski et al.	
	A277*	US-20030077867-A1	04-24-2003	Fitzgerald	
	A278*	US-20030080361-A1	05-01-2003	Murthy et al.	
	A279*	US-20030141548-A1	07-31-2003	Anderson et al.	
	A280*	US-20040007715-A1	01-15-2004	Webb et al.	
	A281*	US-20040110378-A1	06-10-2004	Ghyselen et al.	
	A282*	US-20040173790-A1	09-09-2004	Yeo et al.	
	A283*	US-5,405,802	04-11-1995	Yamagata et al.	
	A284*	US-5,439,843	08-08-1995	Sakaguchi et al.	
	A285*	US-5,705,421	01-06-1998	Matsushita et al.	
	A286*	US-5,821,577	10-13-1998	Crabbe et al.	
	A287*	US-5,855,693	01-05-1999	Murari et al.	
	A288*	US-5,951,757	09-14-1999	Dubbelday et al.	
	A289*	US-6,013,553	01-11-2000	Wallace et al.	
	A290*	US-6,350,311	02-26-2002	Chin et al.	
	A291*	US-6,500,694	12-31-2002	Enquist	
	A292*	US-6,534,380	03-18-2003	Yamauchi et al.	
	A293*	US-6,689,211	02-10-2004	Wu et al.	
	A294*	US-6,790,747-A1	09-14-2004	Henley et al.	
	A295*	US-6,890,835	05-10-2005	Chu et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>5</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>6</sup> (if known)				
	B50	JP-2-210816	08-22-1990		Abstract	✓
	B51	JP-3-036717	02-18-1991			✓
	B52	JP-6-244112	09-02-1994		Abstract only	✓
	B53	JP-6-252046	09-09-1994		Abstract only	✓
	B54	JP-61-141116	06-28-1986		Abstract only	✓

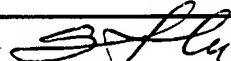
\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. \* CITE NO.: Those application(s) which are marked with an single asterisk (\*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author ( in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	C166	Al-Bayati et al., "Exploring the limits of pre-amorphization implants on controlling channeling and diffusion of low energy B implants and ultra shallow junction formation," 2000 Conf. on Ion Implantation Technology, pp. 54-57.	






Examiner Signature	<i>Shouxiang Hu</i>	Date Considered	10/16/07
-----------------------	---------------------	--------------------	----------

Substitute for form 1449/PTO		<b>Complete if Known</b>			
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		Application Number	10/802,186-Conf. #3869		
		Filing Date	March 17, 2004		
		First Named Inventor	Cheng		
		Art Unit	2811		
		Examiner Name	Shouxiang Hu		
Sheet	2	of	3	Attorney Docket Number	ASC-025DV2C1

C167	Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with sustained epitaxial films", IBM, USA (2002) (abstract).	
C168	Examination Report for European Patent Application No. 01 973 651.1, dated Sept. 7, 2005, 4 pages.	
C169	Examination Report for European Patent Application No. 01 973 651.1-1528, dated March 22, 2004, 3 pages.	
C170	Examination Report for European Patent Application No. 01 973 651.1-1528, dated November 12, 2004, 9 pages.	
C171	Examination Report for European Patent Application No. 01 989 893.1-1235, dated August 16, 2004, 5 pages.	
C172	Examination Report for European Patent Application No. 02 709 406.9-2203, dated March 24, 2005, 5 pages.	
C173	Examination Report for European Patent Application No. 02 709 406.9-2203, dated May 11, 2004, 3 pages.	
C174	Examination Report for European Patent Application No. 98 931 529.6-2203, dated January 10, 2002, 4 pages.	
C175	Examination Report for European Patent Application No. 98 931 529.6-2203, dated May 9, 2003, 5 pages.	
C176	Fitzgerald et al., "Dislocations in Relaxed SiGe/Si Heterostructures," Physica Status Solidi A, Vol. 171, Nr. 1, pg. 227-238, January 16, 1999.	
C177	Grillot et al., "Acceptor diffusion and segregation in (Al <sub>x</sub> Ga <sub>1-x</sub> ) <sub>0.5</sub> In <sub>0.5</sub> P heterostructures," 91 J. Applied Physics 8, April 2002, pp. 4891-4899.	
C178	Halsall et al., "Electron diffraction and Raman studies of the effect of substrate misorientation on ordering in the AlGaInP system," 85 J. Applied Physics 1, Jan. 1999, pp. 199-202.	
C179	Hsu et al., "Surface Morphology of related Ge <sub>x</sub> Si <sub>1-x</sub> films," 61 Appl. Phys. Lett. 11, Sept. 1992, pp. 1293-1295.	
C180	International Search Report for Int'l Application No. PCT/US01/46322, mailed Jan. 22, 2003.	
C181	International Search Report for International Application No. PCT/US2003/18007, January 5, 2004.	
C182	International Search Report for Patent Application No. PCT/US 98/13076, dated October 27, 1998, 2 pages.	
C183	Klauek et al., "Thermal stability of undoped strained Si channel SiGe heterostructures," American Institute of Physics, April 1, 1996, pgs. 1975-1977.	
C184	Kubota M. et al. "New SOI CMOS Process with Selective Oxidation," IEEE IEDM TECH. DIG., pp. 814-816 (1986).	
C185	Ming et al., "Interfacial roughness scaling and strain in lattice mismatched Si <sub>0.4</sub> Ge <sub>0.6</sub> thin films on Si," 67 Applied Physics Letters 5, July 31, 1995, pp. 629-631.	
C186	Ming et al., "Microscopic structure of interfaces in Si <sub>1-x</sub> Ge <sub>x</sub> /Si heterostructures and superlattices studied by x-ray scattering and fluorescence yield," 47 Physical Review B, No. 24, pp. 373-81, June 15, 1993.	
C187	Nishi et al. "Handbook of Semiconductor Manufacturing Technology," Marcel Dekker AG, New York, NY, 2000 pp. 1-22.	
C188	Notice of Final Rejection for Korean Patent Application No. 10-1999-7012279, dated February 25, 2003 2 pages (English translation attached).	
C189	Notice of Preliminary Rejection for Korean Patent Application No. 10-1999-7012279, dated February 21, 2002, 2 pages (English translation attached).	
C190	O'Neill, et al., "Deep Submicron CMOS Based on Silicon Germanium Technology," 43 IEEE Transactions on Electron Devices 6, June 1996 pp. 911-918.	

Examiner Signature		Date Considered	02/16/07
--------------------	---	-----------------	----------

Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	10/802,186-Conf. #3869
				Filing Date	March 17, 2004
				First Named Inventor	Cheng
				Art Unit	2811
				Examiner Name	Shouxiang Hu
Sheet	3	of	3	Attorney Docket Number	ASC-025DV2C1

	C191	Partial International Search Report for International Patent Application No. PCT/US2006/035814, February 7, 2007 (7 pages).	
	C192	Rosenblad et al., "Strain relaxation of graded SiGe buffers grown at very high rates," Materials Science and Engineering B, Vol. 71, Nr. 1-3, pg. 20-23, February 2000.	
	C193	Soderborg, "Fabrication of BESOI-Materials Using Implanted Nitrogen as an Effective Etch Stop Barrier," 1989 IEEE SOS/SOI Technology Conference, pp. 64.	
	C194	Vossen et al. "Thin Film Processes II" Academic Press Inc., San Diego, CA 1991, pp. 370-442.	
	C195	Wolfe et al. "Silicon Processing for the VLSI ERA, Volume 1: Process Technology," Marcel Dekker AG, New York, NY, 2000, pp. 1-35.	

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.  
LIBC/3097311

Examiner Signature		Date Considered	10/16/07
-----------------------	---	--------------------	----------


Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)			<b>Complete if Known</b>		
			Application Number	10/802,186-Conf. #3869	
			Filing Date	March 17, 2004	
			First Named Inventor	Cheng	
			Art Unit	2811	
			Examiner Name	Shouxiang Hu	
Sheet	1	of	3	Attorney Docket Number	ASC-025DV2C1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	A275*	US-20020167048-A1	11-14-2002	Tweet et al.	
	A276*	US-20030027381-A1	02-06-2003	Buynoski et al.	
	A277*	US-20030077867-A1	04-24-2003	Fitzergald	
	A278*	US-20030080361-A1	05-01-2003	Murthy et al.	
	A279*	US-20030141548-A1	07-31-2003	Anderson et al.	
	A280*	US-20040007715-A1	01-15-2004	Webb et al.	
	A281*	US-20040110378-A1	06-10-2004	Ghyselen et al.	
	A282*	US-20040173790-A1	09-09-2004	Yeo et al.	
	A283*	US-5,405,802	04-11-1995	Yamagata et al.	
	A284*	US-5,439,843	08-08-1995	Sakaguchi et al.	
	A285*	US-5,705,421	01-06-1998	Matsushita et al.	
	A286*	US-5,821,577	10-13-1998	Crabbe' et al.	
	A287*	US-5,855,693	01-05-1999	Murari et al.	
	A288*	US-5,951,757	09-14-1999	Dubbelday et al.	
	A289*	US-6,013,553	01-11-2000	Wallace et al.	
	A290*	US-6,350,311	02-26-2002	Chin et al.	
	A291*	US-6,500,694	12-31-2002	Enquist	
	A292*	US-6,534,380	03-18-2003	Yamauchi et al.	
	A293*	US-6,689,211	02-10-2004	Wu et al.	
	A294*	US-6,790,747-A1	09-14-2004	Henley et al.	
	A295*	US-6,890,835	05-10-2005	Chu et al.	

























FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)				
	B50	JP-2-210816	08-22-1990		Abstract	✓
	B51	JP-3-036717	02-18-1991			✓
	B52	JP-6-244112	09-02-1994		Abstract only	✓
	B53	JP-6-252046	09-09-1994		Abstract only	✓
	B54	JP-61-141116	06-28-1986		Abstract only	✓

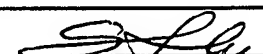
\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. \* CITE NO.: Those application(s) which are marked with an single asterisk (\*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author ( in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	C166	Al-Bayati et al., "Exploring the limits of pre-amorphization implants on controlling channeling and diffusion of low energy B implants and ultra shallow junction formation," 2000 Conf. on Ion Implantation Technology, pp. 54-57.	



Examiner Signature		Date Considered	02/16/07
--------------------	---	-----------------	----------

Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>		<b>Complete if Known</b>			
		Application Number	10/802,186-Conf. #3869		
		Filing Date	March 17, 2004		
		First Named Inventor	Cheng		
		Art Unit	2811		
		Examiner Name	Shouxiang Hu		
Sheet	2	of	3	Attorney Docket Number	ASC-025DV2C1

	C167	Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with sustained epitaxial films", IBM, USA (2002) (abstract).	
	C168	Examination Report for European Patent Application No. 01 973 651.1, dated Sept. 7, 2005, 4 pages.	
	C169	Examination Report for European Patent Application No. 01 973 651.1-1528, dated March 22, 2004, 3 pages.	
	C170	Examination Report for European Patent Application No. 01 973 651.1-1528, dated November 12, 2004, 9 pages.	
	C171	Examination Report for European Patent Application No. 01 989 893.1-1235, dated August 16, 2004, 5 pages.	
	C172	Examination Report for European Patent Application No. 02 709 406.9-2203, dated March 24, 2005, 5 pages.	
	C173	Examination Report for European Patent Application No. 02 709 406.9-2203, dated May 11, 2004, 3 pages.	
	C174	Examination Report for European Patent Application No. 98 931 529.6-2203, dated January 10, 2002, 4 pages.	
	C175	Examination Report for European Patent Application No. 98 931 529.6-2203, dated May 9, 2003, 5 pages.	
	C176	Fitzgerald et al., "Dislocations in Relaxed SiGe/Si Heterostructures," Physica Status Solidi A, Vol. 171, Nr. 1, pp. 227-238, January 16, 1999.	
	C177	Grillot et al., "Acceptor diffusion and segregation in (Al <sub>x</sub> Ga <sub>1-x</sub> ) <sub>0.5</sub> In <sub>0.5</sub> P heterostructures," 91 J. Applied Physics 8, April 2002, pp. 4891-4899.	
	C178	Halsall et al., "Electron diffraction and Raman studies of the effect of substrate misorientation on ordering in the AlGaInP system," 85 J. Applied Physics 1, Jan. 1999, pp. 199-202.	
	C179	Hsu et al., "Surface Morphology of related Ge <sub>x</sub> Si <sub>1-x</sub> films," 61 Appl. Phys. Lett. 11, Sept. 1992, pp. 1293-1295.	
	C180	International Search Report for Int'l Application No. PCT/US01/46322, mailed Jan. 22, 2003.	
	C181	International Search Report for International Application No. PCT/US2003/18007, January 5, 2004.	
	C182	International Search Report for Patent Application No. PCT/US 98/13076, dated October 27, 1998, 2 pages.	
	C183	Klauk et al., "Thermal stability of undoped strained Si channel SiGe heterostructures," American Institute of Physics, April 1, 1996, pgs. 1975-1977.	
	C184	Kubota M. et al. "New SOI CMOS Proess with Selective Oxidation," IEEE IEDM TECH. DIG., pp. 814-816 (1986).	
	C185	Ming et al., "Interfacial roughness scaling and strain in lattice mismatched Si <sub>0.4</sub> Ge <sub>0.6</sub> thin films on Si," 67 Applied Physics Letters 5, July 31, 1995, pp. 629-631.	
	C186	Ming et al., "Microscopic structure of interfaces in Si <sub>1-x</sub> Ge <sub>x</sub> /Si heterostructures and superlattices studied by x-ray scattering and fluorescence yield," 47 Physical Review B, No. 24, pp. 373-81, June 15, 1993.	
	C187	Nishi et al. "Handbook of Semiconductor Manufacturing Technology," Marcel Dekker AG, New York, NY, 2000 pp. 1-22.	
	C188	Notice of Final Rejection for Korean Patent Application No. 10-1999-7012279, dated February 25, 2003 2 pages (English translation attached).	
	C189	Notice of Preliminary Rejection for Korean Patent Application No. 10-1999-7012279, dated February 21, 2002, 2 pages (English translation attached).	
	C190	O'Neill, et al., "Deep Submicron CMOS Based on Silicon Germanium Technology," 43 IEEE Transactions on Electron Devices 6, June 1996 pp. 911-918.	

Examiner Signature		Date Considered	10/16/07
--------------------	---	-----------------	----------

Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	10/802,186-Conf. #3869
				Filing Date	March 17, 2004
				First Named Inventor	Cheng
				Art Unit	2811
				Examiner Name	Shouxiang Hu
Sheet	3	of	3	Attorney Docket Number	ASC-025DV2C1

	C191	Partial International Search Report for International Patent Application No. PCT/US2006/035814, February 7, 2007 (7 pages).	
	C192	Rosenblad et al., "Strain relaxation of graded SiGe buffers grown at very high rates," Materials Science and Engineering B, Vol. 71, Nr. 1-3, pg. 20-23, February 2000.	
	C193	Soderbarg, "Fabrication of BESOI-Materials Using Implanted Nitrogen as an Effective Etch Stop Barrier," 1989 IEEE SOS/SOI Technology Conference, pp. 64.	
	C194	Vossen et al. "Thin Film Processes II" Academic Press Inc., San Diego, CA 1991, pp. 370-442.	
	C195	Wolfe et al. "Silicon Processing for the VLSI ERA, Volume 1: Process Technology," Marcel Dekker AG, New York, NY, 2000, pp. 1-35.	

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.  
LIBC/3097311

Examiner Signature		Date Considered	10/16/07
--------------------	---	-----------------	----------